

WHAT IS CLAIMED IS:

1 A media processing system, comprising:
2 DRAM having a plurality of storage locations for storing digital data being
3 processed by said media processing system, said digital data including video data that is
4 compressed in a standardized format;
5 means for processing said digital data that includes said standardized
6 format compressed video data to produce compressed video images and image data;
7 means for decoding said standardized format compressed video images to
8 generate full motion video pixel data;
9 means for sharing said DRAM between said processing means and said
10 decoding means; and
11 means for producing a full motion video signal from said full motion video
12 pixel data.

1 2. The system as recited in claim 1, wherein said compressed video
2 data comprises a plurality of pixels, and said standardized compressed format comprises a
3 luminance sample generated for each pixel, and two chrominance samples generated for
4 every four pixels.

1 3. The system as recited in claim 2, wherein said decoding means
2 comprises a Motion Picture Expert Group decoder.

1 4. The system as recited in claim 1, wherein said compressed video
2 data comprises a plurality of pixels, and said processing means comprises means for
3 multiplying a first pixel with a second pixel in a single clock cycle of said processing
4 means.

1 5. The system as recited in claim 4, wherein said pixels have a first
2 portion, a second portion and a third portion, and said means for multiplying pixels
3 comprises means for multiplying a portion of the first pixel with a corresponding portion
4 of the second pixel.

1 6. The system as recited in claim 1, wherein said compressed video
2 data comprises a plurality of pixels, and said processing means comprises means for

3 combining a first pixel with a second pixel in a single clock cycle of said processing
4 means.

1 7. The system as recited in claim 6, wherein said pixels have a first
2 portion, a second portion and a third portion, and said means for combining pixels
3 comprises means for combining a portion of the first pixel with a corresponding portion
4 of the second pixel.

5 8. The system as recited in claim 1, wherein said processing means
6 comprises a plurality of processing elements connected together in parallel, means for
7 controlling said processing elements with instruction words that have a predetermined
8 number of instructions, and means for distributing data simultaneously to each of said
9 processing elements.

1 9. The system as recited in claim 8, wherein said processing elements
2 comprise a plurality of processing units wherein each of said processing units is
3 controlled by one of said predetermined number of instructions.

4 10. The system as recited in claim 1, wherein said DRAM stores audio
5 data that is compressed in a standardized format, and further comprising means for
6 decompressing said audio data that is compressed in a standardized format to generate
7 uncompressed audio data, and means for combining said full-motion video data and said
8 uncompressed audio data to generate full-motion multimedia data.

9 11. The system as recited in claim 9, wherein said processing units
10 comprise a plurality of storage locations within said processing units, each storage
11 location having a predetermined physical size, and means for combining said storage
12 locations together to form a storage location that stores data that is larger than the
13 predetermined physical size of each storage location.

14 12. A single semiconductor chip media processor, comprising:
15 a semiconductor memory, internal to said single semiconductor chip, for
16 storing digital data, including video digital data compressed in standardized format;
17 means for processing said compressed video data in said semiconductor
18 memory to produce color, full motion video data that is temporarily stored in said
19 semiconductor memory;

7 means for decoding said color, full motion video data stored in said
8 semiconductor memory to generate color, full motion video image data; and
9 means for producing a color, full motion video image signal.

1 13. The processor as recited in claim 12, wherein said compressed
2 video data comprises a plurality of pixels, and said processing means comprises means
3 for multiplying a first pixel with a second pixel in a single clock cycle of said processing
4 means.

1 14. The processor as recited in claim 13, wherein said pixels have a
2 first portion, a second portion and a third portion, and said means for multiplying pixels
3 comprises means for multiplying a portion of the first pixel with a corresponding portion
4 of the second pixel.

1 15. The processor as recited in claim 14, wherein said compressed
2 video data comprises a plurality of pixels, and said processing means comprises means
3 for combining a first pixel with a second pixel in a single clock cycle of said processing
4 means.

1 16. The processor as recited in claim 15, wherein said pixels have a
2 first portion, a second portion and a third portion, and said means for combining pixels
3 comprises means for combining a portion of the first pixel with a corresponding portion
4 of the second pixel.

1 17. The processor as recited in claim 12, wherein said processing
2 means comprises a plurality of processing elements connected together in parallel, means
3 for controlling said processing elements with instruction words that have a predetermined
4 number of instructions, and means for distributing data simultaneously to each of said
5 processing elements.

1 18. The processor as recited in claim 17, wherein said processing
2 elements comprise a plurality of processing units wherein each of said processing units is
3 controlled by one of said predetermined number of instructions.

1 19. The processor as recited in claim 12, wherein said DRAM stores
2 audio data that is compressed in a standardized format, and further comprising means for

3 decompressing said audio data that is compressed in a standardized format to generate
4 uncompressed audio data, and means for combining said full-motion video data and said
5 uncompressed audio data to generate full-motion multimedia data.

1 20. The processor as recited in claim 18, wherein said processing units
2 comprise a plurality of storage locations within said processing units, each storage
3 location having a predetermined physical size, and means for combining said storage
4 locations together to form a storage location that stores data that is larger than the
5 predetermined physical size of each storage location.

1 21. A method of processing media, comprising:
2 storing digital data being processed by said media processing system in a
3 DRAM, said digital data including video data that is compressed in a standardized format;
4 processing said digital data that includes said standardized format
5 compressed video data to produce compressed video images and image data;
6 decoding said standardized format compressed video images to generate
7 full motion video pixel data;
8 sharing said DRAM between said processing means and said decoding
9 means; and
10 producing a full motion video signal from said full motion video pixel
11 data.

1 22. The method as recited in claim 20, wherein said compressed video
2 data comprises a plurality of pixels, and processing comprises multiplying a first pixel
3 with a second pixel in a single clock cycle.

1 23. The method as recited in claim 21, wherein said compressed video
2 data comprises a plurality of pixels, and processing comprises combining a first pixel
3 with a second pixel in a single clock cycle.